

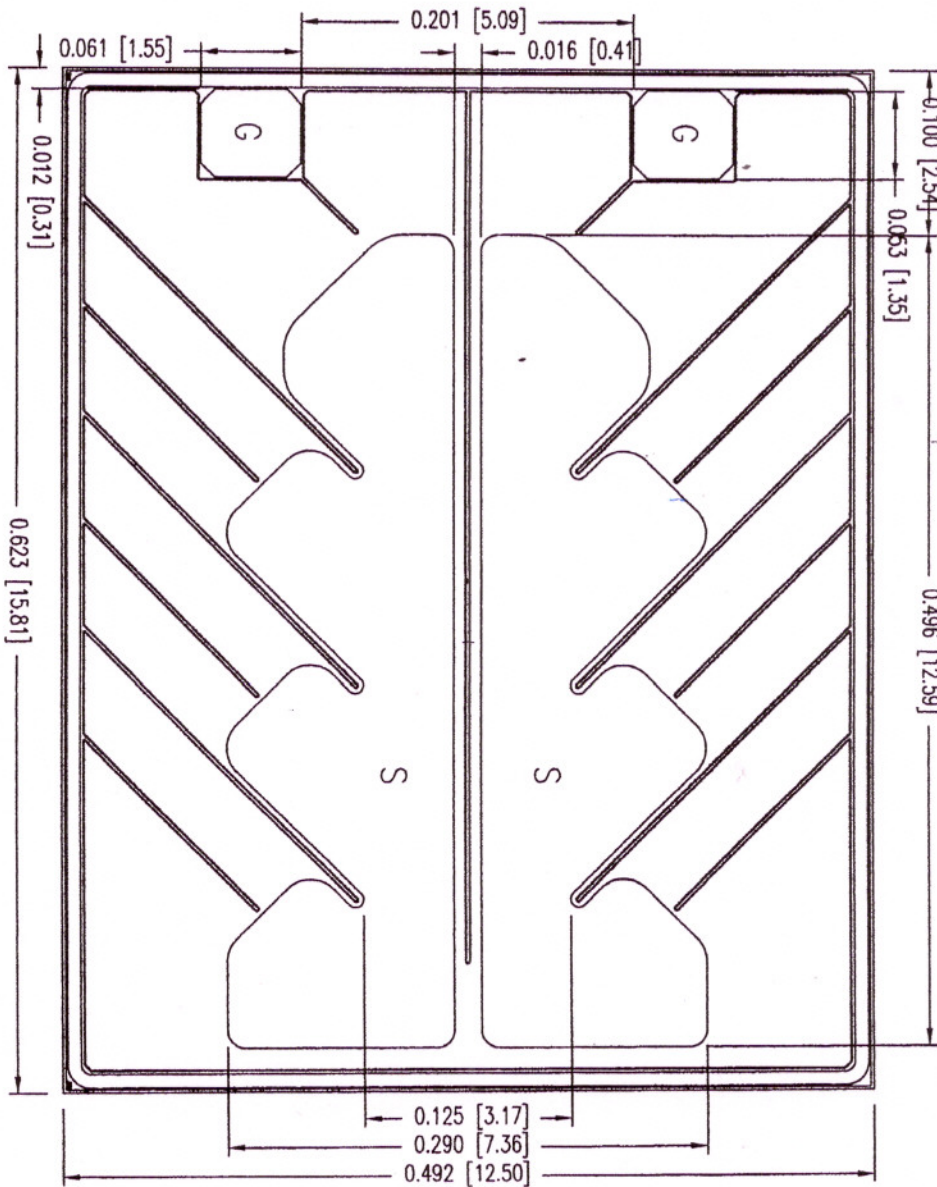


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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



NOTE:

1. DIE DIMENSION:
15.814 x 12.502 mm
[0.6226 x 0.4922"]
2. DIE THICKNESS:
200um±25um
[0.008 ±0.001"]
3. TOP BONDING PAD METAL:
3.0 um NOMINAL THICK
ALUMINUM
4. BACK METAL:
3 LAYERS OF Ti, Ni, Ag
2500Å NOMINAL THICK
SILVER
5. DIE SIZE TOLERANCE
AFTER SAW:
±25um [±0.001"]
6. G = GATE
S = SOURCE
D = DRAIN
(Bottom side of die)

APPROVED BY: MG

DIE SIZE : 623 mils x 492 mils

DATE: 3/7/12

MFG: IXYS

THICKNESS: 8 mils

P/N: IXFD110N60P3